



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: SOUK, Jun-Hyung; LEE, Jeong-Young; YOON, Jong-Soo; CHOI, Kwon-Young; and BAEK, Bum-Ki

Assignee: Samsung Electronics Co., Ltd.

Title: THIN FILM TRANSISTOR ARRAY PANEL AND
MANUFACTURING METHOD THEREOF

Application No.: 10/759,389 Filing Date: 01/16/2004

Examiner: Ton, Minh Toan T. Group Art Unit: 2871

Docket No.: AB-1351 US Confirmation No.: 6707

San Jose, California
April 26, 2006

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

In response to the Advisory Action of May 16, 2006, Applicant requests review of the rejections in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the Remarks below.

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REMARKS

Claims 1-29 were previously pending in the application. In the Response to Final Office Action filed on February 28, 2006, claims 1-14 and 20-24 were canceled, leaving claims 15-19 and 25-29 under consideration.

Claim Rejections Under 35 U.S.C. § 102

In the Final Office Action dated December 29, 2005, the Examiner rejected claim 1 as being anticipated by Akamatsu et al. (U.S. Pat. No. 6,414,730). In the Response to Final Office Action filed on February 28, 2006, claim 1 was canceled, thereby making moot the Examiner's rejection under § 102.

In the Advisory Action dated March 16, 2006, the Examiner failed to indicate whether the proposed cancellation of claim 1 will be entered. Applicant submits that the cancellation of claim 1 should be entered and the rejection of claim 1 under § 102 should be withdrawn.

Claim Rejections Under 35 U.S.C. § 103(a)

The Examiner has rejected claims 2-5 and 15-29 as being unpatentable over the Akamatsu reference as applied to claim 1.

As described above, Applicant requested cancellation of claims 2-5 and 20-24 in the Response to Final Office Action filed on February 28, 2006. Applicant submits that the cancellation of claims 2-5 and 20-24 should be entered and the rejection of claims 2-5 and 20-24 under § 103 should be withdrawn.

Accordingly, claims 15-19 and 25-29 should remain under consideration. In the Advisory Action, the Examiner states, in part:

The request for reconsideration has been considered but does NOT place the application in condition for allowance because: . . . the arguments are found not persuasive. Akamatsu discloses the device comprising the pixel electrode contacting an upper surface of the

gate insulating layer (see at least Figure 2A) and a first contact hole exposing a portion of an upper surface of the gate insulating layer (also see at least Figure 2A). Thus, the final rejection stands.

Applicants respectfully traverse the Examiner's rejection. Claim 15 recites, in part:

a passivation layer formed on the data line and the drain electrode and having a first contact hole exposing the drain electrode at least in part and a portion of an upper surface of the gate insulating layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole.

(Emphasis added.)

Applicants submit that the Examiner has failed to provide any support for modifying the Akamatsu reference to provide a structure having "a first contact hole exposing the drain electrode at least in part and a portion of an upper surface of the gate insulating layer" and a pixel electrode contacting "the exposed portion of the gate insulating layer through the first contact hole", as recited in claim 15. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness.

Contrary to the Examiner's assertion, Figure 2A of the Akamatsu reference fails to teach or suggest the claimed structure. As can be seen in Figure 2A, the through hole 87 does not expose an upper surface of the gate insulation film 53. Instead, Figure 2A shows that the through hole 87 exposes an upper surface of one end 59b of the drain extraction electrode 59. The pixel electrode 69 is connected to the drain extraction electrode 59 via the through hole 87. The Examiner has failed to provide any indication of how Figure 2A discloses the exposing a portion of the upper surface of the gate insulation layer.

Applicants respectfully request that due to the Examiner's clear error the panel reverse the rejection under 35 U.S.C. § 103 of claim 15 and claims 16-19, which depend from claim 15, and allow the claims.

Claim 25 recites, in part:

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole, wherein the pixel electrode contacts an upper surface of the gate insulating layer. (Emphasis added.)

As described above with respect to claim 15, the Examiner has failed to provide any support for how the Akamatsu reference discloses the claimed structure in which the pixel electrode contacts an upper surface of the gate insulating layer, as recited in claim 25. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness and the Examiner's rejection is unsupported.

Applicants respectfully request that due to the Examiner's clear error the panel reverse the rejection under 35 U.S.C. § 103 of claim 25 and claims 26-29, which depend from claim 25, and allow the claims.

Double Patenting

Claims 1-5 have been rejected under the judicially-created doctrine of obviousness-type double patenting over claims of U.S. Publication No. 2005/0030440 to Lee et al.

As described above, Applicant requested cancellation of claims 1-5 in the Response to Final Office Action filed on February 28, 2006. Applicant submits that the cancellation of claims 1-5 should be entered and the rejection of claims 1-5 for double patenting should be withdrawn.



CONCLUSION

If the members of the Review Panel have any questions regarding the above, the undersigned Attorney for Applicants may be reached at (408) 392-9250.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 26, 2006.

H. Matsubayashi

Attorney for Applicant(s)

4/26/2006

Date of Signature

Respectfully submitted,

H. Matsubayashi

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